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DATA INTEGRATION AND COLLECTION ENVIRONMENT (DICE) SYSTEM FIRMWARE SUPPORT MANUAL

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13. ABSTRACT *(Maximum 200 words)*
The major goal of the Data Integration and Collection Environment (DICE) program was to develop a flightworthy prototype of an on-board instrumentation system capable of collecting pertinent data from and embedded information system. The target platform was the F-15 APG-63 radar.

14. SUBJECT TERMS
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Table of Contents

1. SCOPE

1.1 Identification

The Data Integration and Collection Environment (DICE) is an embedded computer based digital data recorder system supporting the F-15 APG-63 radar. This document shall describe the procedures for pre-programming all DICE resident firmware.

1.2 System Overview

The DICE system is a Versa Module Europe (VME) based digital data collection environment comprised of commercial off-the-shelf (COTS), government furnished equipment (GFE), and TRW custom designed hardware and firmware. It captures real time radar data directly from the APG-63 data buses, formats the data, and stores it on digital tape for later analysis.

1.3 Document Overview

This document shall outline those procedures necessary to program each of the pre-programmed circuit card assemblies (CCA) resident in the DICE system chassis. Each CCA will be listed individually with a brief description of the type of programming required. For example, the central processing unit (CPU) card contains the embedded computer program controlling all system functions, but the TRW custom card firmware contains the data files required to configure field programmable gate arrays (FPGAs).

2. REFERENCED DOCUMENTS

2.1 Government Documents

The following documents of the exact issue shown form a part of this document to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this document, the contents of this document shall be considered a superseding requirement.

SPECIFICATIONS

None.

STANDARDS

MIL-STD-883E	Test Method Standard, Microcircuits, 1996

DRAWINGS

None.

OTHER DOCUMENTS

None.

Copies of specifications, standards, drawings, and publications required by suppliers in connection with specified procurement functions should be obtained from the contracting agency or as directed by the contracting officer.

2.2 Non-Government Documents

The following documents of the exact issue shown form a part of this document to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this document, the contents of this document shall be considered a superseding requirement.

SPECIFICATIONS

Nov 1990	PMV 68 ICP-2 Specification, Issue A, Publication No. 681/SA/04079

STANDARDS

None.

DRAWINGS

834783	H009 FPGA1
834784	H009 FPGA2

834785	H009 FPGA3
834786	H009 FPGA4
834791	PSP FPGA1
834792	PSP FPGA2
834793	PSP FPGA3

OTHER DOCUMENTS

YN68104323-x07 Jan 1994	Software Application Note, PMV68 ICP-2 Programming Software

Technical society and technical association specifications and standards are generally available for reference from libraries. They are also distributed among technical groups and using Federal Agencies.

3. FIRMWARE DEVICE INFORMATION

The following paragraphs shall describe each of the pre-programmed firmware devices resident in the DICE system.

3.1 Device Description

The following paragraphs shall describe each of the individual CCAs by manufacturer, and their firmware programming requirements.

3.1.1 CPU-3A CCA

The CPU-3A is a Radstone Technology 68030 based, VMEbus single board computer. This CCA has 32Kbytes by 8 bits wide boot/configuration electrically erasable programmable read only memory (EEPROM). This memory contains processor and system dependent variables, as well as boot firmware to reprogram the main electrically programmable read only memory (EPROM) using the ICP-2. The procedure for this programming function is outlined in paragraph 4 of this document.

The DICE system firmware resides in main EPROM organized as 2Mbyte by 32 bit wide EPROM.

3.1.2 H009 Interface CCA

The H009 Interface CCA is a TRW custom designed circuit card (PN 834780) residing in the A1A4 slot of the DICE system chassis. Although it has no microprocessor memory, its digital logic implementation makes extensive use of Xilinx FPGAs. These FPGAs are Static Random Access Memory (SRAM) based, which means that they maintain their configuration only while power is applied and a configuration file has been loaded. The devices become blank when power is removed. Therefore, individual FPGAs must be reloaded with configuration data each time power is applied to the board. This is accomplished by loading the configuration files into a serial EPROM installed on the CCA. When power is applied the FPGA boots up from the EPROM data to its desired configuration. Each FPGA requires its own configuration EPROM.

The H009 Interface CCA has four Xilinx XC3042 FPGAs and four configuration EPROMs. Each of the EPROMs contains the configuration data which is graphically illustrated by the individual FPGA schematic diagrams (TRW Dwg Nos. 834783, 834784, 834785, 834786).

3.1.3 Programmable Signal Processor (PSP) Interface CCA

The PSP Interface CCA is a TRW custom designed circuit card (PN 834788) residing in the A1A3 slot of the DICE system chassis. The digital logic implementation of this circuit card makes extensive use of Xilinx FPGAs. These FPGAs are SRAM based, which means that they maintain their configuration only while power is applied and a configuration file has been loaded. The devices become blank when power is removed. Therefore, individual FPGAs must be reloaded with configuration data each time power is applied to the board. This is accomplished by loading the configuration files into a serial EPROM installed on the CCA.

When power is applied the FPGA boots up from the EPROM data to its desired configuration. Each FPGA requires its own configuration EPROM.

The PSP Interface CCA has three Xilinx 4000 series FPGAs and five configuration EPROMs. These include two Xilinx XC4010 FPGAs and one XC4005. Each XC4010 requires two configuration EPROMs plus one EPROM for the XC4005.

The design of the PSP Interface card contains extensive built-in test (BIT) circuitry. The BIT test vectors are stored in read only memory (ROM) areas embedded within the FPGA program file. Therefore, no additional programming requirements are needed for this CCA.

Each of the EPROMs contains the configuration data which is graphically illustrated by the individual FPGA schematic diagrams (TRW Dwg Nos. 834791, 834792, 834793).

3.2 Installation and Repair Procedures

All CCAs described above contain static sensitive components and Electrostatic Discharge (ESD) procedures should be observed at all times these cards are handled. The military version of the CPU-3A card contains EPROM modules. These modules cannot be removed and erasure requires an Ultra Violet (UV) eraser capable of supporting the 6U VME form factor. Because the EPROM modules are not socketed, they must be programmed in circuit as well.

The TRW custom interface cards (H009 and PSP) were designed to meet flight requirements and do not contain any socketed components. The FPGA configuration EPROMs are programmed externally and soldered to the circuit board. These serial EPROMs are one-time programmable, and any failure or configuration change would require a new EPROM to be burned.

3.3 Security

None of the DICE system hardware, software, or firmware contains classified information. Any classified data that may be collected during a mission would be stored on digital tape which can be removed from the system and handled accordingly. All DICE data buffers that may temporarily store classified data are SRAM based memories and the information is destroyed when system power is removed.

3.4 Limitations

All DICE hardware is designed to operate in an aircraft environment. All subassemblies are ruggedized to meet appropriate military standards, and all firmware devices used on both COTS and TRW custom subassemblies were chosen to meet MIL-STD 883B specifications.

4. PROGRAMMING EQUIPMENT AND PROCEDURES

The following paragraphs describe the hardware and software necessary to program all DICE firmware.

4.1 Programming Hardware

Two different programming methodologies are required for the DICE system firmware. The TRW custom boards (H009 and PSP interfaces) require any IBM PC clone (80386 or greater) and the Logical Devices Allpro 88 universal device programmer. The Logical Devices hardware includes an interface card mounted in a spare slot of the PC and an interface cable installed between the PC card and the Allpro. Almost any device programmer is sufficient, but the programming procedures developed in this document assume the Logical Devices Allpro 88.

The Radstone Technology CPU-3A board requires an IBM PC clone, the DICE system VME chassis, a serial cable with 15-pin D connector, the Radstone Technology PMV 68 ICP-2 in-circuit programming card, and the programming cable included with the PMV 68 ICP-2 card. A UV eraser of sufficient size to accept the 6U VME form factor is required to erase the EPROM. The military version of this circuit card does not contain socketed memory components. Therefore the entire board must be placed in the eraser.

4.2 Programming Software

The programming software required for the H009 and PSP Interface cards consists of the Logical Devices Allpro software version V2.70. The programming procedures assume DOS 5.0 or greater is resident on the PC and that the Xilinx configuration data files have already been generated. The following paragraphs outline programming procedures for using deliverable media and do not include procedures for generation of the design files.

The CPU 3-A card uses the PC as a host and communicates with it via the serial interface. The programming software is included with the PMV 68 ICP-2 card (Radstone Technology P/N 681-1-04323-100) in floppy disk DOS format. The PROM-based Local Universal Monitor (PLUM) software is resident on the CPU 3-A card in the boot/utility EEPROM memory space, and is used to communicate with the PC during the programming process. The PMV 68 ICP-2 card provides the programming voltage and timing pulses to the CPU-3A via the programming cable.

4.3 Loading Procedures

The loading/burning procedures for all DICE system pre-programmed firmware is outlined in the following paragraphs.

4.3.1 CPU-3A CCA

The CPU-3A CCA contains UV erasable EPROM and EEPROM which require programming. This is accomplished using the PMV 68 ICP-2 card installed in the VME chassis and by downloading the program files from the host PC.

1) Prior to programming, the EPROM must be erased. Remove the CPU-3A card from the VME chassis and ensure the protective covering is removed from the EPROM modules to allow exposure to the UV light.

2) Then place the entire board into the UV eraser and set the exposure time to approximately 45 minutes.

3) After the erasure is complete, remove the CPU-3A card from the eraser. Remove link 6 from the card and reinstall it in slot 1 of the VME chassis. Removal of this jumper enables the EPROM on the CPU-3A for programming.

4) Install the PMV 68 ICP-2 card in the next available card slot of the VME chassis.

5) Connect the serial cable between the PC serial port and the 15-pin D connector on the front of the CPU-3A card. Connect the programming cable between the 15-pin D connector on the PMV 68 ICP-2 card and the 10-pin header (P4) on the CPU-3A card.

6) Apply power to the PC and the VME chassis and wait for the menu to appear on the PC screen. The menu should be similar to the following:

PMV 68 ICP-2 Programming Software.

Options are:

1. Download Programming Software.
2. Execute Programming Software.
3. Quit.

7) Select option 1 to download the data file in Motorola S-Record format from the PC to RAM area of the CPU-3A card. When the download is complete the user will be prompted to "Hit Return" to return to the main menu.

8) At the main menu, select option 2 to begin execution of the programming software. Selecting this option causes a new menu appear with the following options available:

PMV 68 ICP-2 Programming Software

Options available are:

1. Perform Checksum Only.
2. Perform Verification of Data Only.
3. Perform Blank Test, Programming, Verification, and Checksum of EPROM.
4. Perform Programming, Verification and Checksum of EEPROM.
5. Download Programming Data from Host.
0. Quit.

9) Select option 3 from the menu and follow the prompts. Refer to Radstone Technology manual PMV 68 ICP-2 Specification for detailed information. If the blank check fails, a

message is displayed and the CPU-3A card must be removed from the chassis and the erasure steps 1 - 3 must be repeated.

10) Before EPROM programming commences, the software will prompt the user to set the programming switch on the PMV 68 ICP-2 front panel. This switch enables the programming voltages to be output to the CPU-3A card. Once set, a programming message is displayed on the screen indicating progress.

11) When the programming complete message is displayed, reset the programming voltage switch on the PMV 68 ICP-2 card.

12) When the software detects that the switch has been reset, a verification of the load is initiated and a checksum is calculated. The results are displayed on the PC terminal. At completion, press "Return" to return to the main menu.

13) Power down the VME chassis and the PC. Remove the CPU-3A card and reinstall link 6. This link must be installed for EEPROM programming and for normal operation. It is removed only for EPROM programming.

14) Repeat steps 4 - 7 and select option 4 from the programming menu to program the EEPROM memory. Follow the messages displayed on the terminal. The following messages should be displayed:

Programming.....

Perform Checksum Only.

Programming complete.

Verification complete.

Checksum =

Press return to continue.

15) Press "Return" to return to the main menu. Programming of the CPU-3A card is now complete. The VME chassis and the PC may be turned off.

4.3.2 H009 Interface CCA

This procedure consists of programming four serial EPROMs corresponding to the four XC3042 FPGAs used on the H009 Interface CCA.

1) Turn on the PC and the Allpro 88 device programmer.

2) Place the blank Xilinx EPROM in the Allpro programming Zero Insertion Force (ZIF) socket taking care to observe the orientation mark to the side of the socket. Place the ZIF lock arm to the "down" position to lock the device into the socket.

3) Change the directory of the PC to c:\allpro.

4) Type allpro to invoke the Allpro menu driven software.

5) Select the appropriate device type and library (PRMXLX).

6) Use the arrow keys to select the device part number (XC1736D).

7) Select "Blank Check" from the programming menu to ensure the device to be programmed is blank. These EPROMs are one time programmable and if it is not blank, a different one must be selected.

8) Select "Read Formatted File" from the programming menu. Then select Intel Hex format to load the PROM file into Allpro memory. The full path and filename to be loaded must be specified. The filename should be of the format *<filename>*.mcs. Choose the first of the four files to be programmed.

9) Select "Program Device" from the programming menu. The red light on the Allpro illuminates while device access is occurring. When the device has successfully been programmed and verified, the red light will extinguish and the green light will be lit.

10) Note the checksum displayed to ensure proper installation for each FPGA. Raise the ZIF socket handle to the "up" position and remove the programmed device.

11) Repeat steps 2 - 10 for the remaining three EPROMs to be programmed.

4.3.3 PSP Interface CCA (XC4005 Programming Procedures)

This procedure consists of programming one serial EPROM corresponding to the one Xilinx XC4005 FPGA used on the PSP Interface CCA. The XC4005 requires one EPROM while the XC4010 FPGAs require two programmed EPROMs each. The procedures below will address the XC4005 (single PROM programming). The XC4010 programming procedures will be addressed in paragraph 4.3.4.

1) Turn on the PC and the Allpro 88 device programmer.

2) Place the blank Xilinx EPROM in the Allpro programming ZIF socket taking care to observe the orientation mark to the side of the socket. Place the ZIF lock arm to the "down" position to lock the device into the socket.

3) Change the directory of the PC to c:\allpro.

4) Type allpro to invoke the Allpro menu driven software.

5) Select the appropriate device type and library (PRMXLX).

6) Use the arrow keys to select the device part number (XC17128D).

7) Select "Blank Check" from the programming menu to ensure the device to be programmed is blank. These EPROMs are one time programmable and if it is not blank, a different one must be selected.

8) Select "Read Formatted File" from the programming menu. Then select Intel Hex format to load the PROM file into Allpro memory. The full path and filename to be loaded must be specified. The filename should be of the format *<filename>*.mcs. Choose the file to be programmed.

9) Select "Program Device" from the programming menu. The red light on the Allpro illuminates while device access is occurring. When the device has successfully been programmed and verified, the red light will extinguish and the green light will be lit.

10) Note the checksum displayed to ensure proper installation for each FPGA. Raise the ZIF socket handle to the "up" position and remove the programmed device.

4.3.4 PSP Interface CCA (XC4010 Programming Procedures)

This procedure consists of programming four serial EPROMs corresponding to the two Xilinx XC4010 FPGAs used on the PSP Interface CCA. The XC4010 FPGAs require two programmed EPROMs each. The procedures below will address the XC4010 (dual PROM programming).

1) Turn on the PC and the Allpro 88 device programmer.
2) Place the blank Xilinx EPROM in the Allpro programming ZIF socket taking care to observe the orientation mark to the side of the socket. Place the ZIF lock arm to the "down" position to lock the device into the socket.
3) Change the directory of the PC to c:\allpro.
4) Type allpro to invoke the Allpro menu driven software.
5) Select the appropriate device type and library (PRMXLX).
6) Use the arrow keys to select the device part number (XC17128D).
7) Select "Blank Check" from the programming menu to ensure the device to be programmed is blank. These EPROMs are one time programmable and if it is not blank, a different one must be selected.
8) Select "Read Formatted File" from the programming menu. Then select Intel Hex format to load the PROM file into Allpro memory. The full path and filename to be loaded must be specified. The filename should be of the format *<filename>*.mcs. Choose the first of the four files to be programmed.
9) The next screen is the Download Parameter Editor. The information should be entered as follows:

   # of Devices in Set..... 1 (default)

   Current Device ..... 0 (default)

   Start File Address ..... 0 (default)

   End File Address ..... 3fff (for the first of two)

   Start Device Address ..... 0 (default)

   Nibble to Download..... 2

10) Select F10 when done.
11) Select "Program Device" from the programming menu. The red light on the Allpro illuminates while device access is occurring. When the device has successfully been programmed and verified, the red light will extinguish and the green light will be lit.
12) Note the checksum displayed to ensure proper installation for each FPGA. Raise the ZIF socket handle to the "up" position and remove the programmed device.

13) Place the second blank EPROM into the Allpro and follow steps 5 - 8 above.

14) At the Download Parameter Editor screen, enter the programming information as shown below.

# of Devices in Set..... 1 (default)

Current Device ..... 0 (default)

Start File Address ..... 4000 (for second of two)

End File Address ..... 7fff (for the second of two)

Start Device Address ..... 0 (default)

Nibble to Download..... 2

15) Repeat steps 1 - 14 to complete the programming process for the second XC4010 EPROM set.

5. VENDOR INFORMATION

The documents listed below contain detailed data sheets and further programming specifications for all firmware components used in the DICE system.

For Xilinx FPGA vendor information:

The Programmable Logic Book, 1994

Xilinx

2100 Logic Drive

San Jose, CA 95124

For Radstone Technology vendor information:

PMV 68 ICP-2 Specification

Radstone Technology Corp.

20 Craig Road

Montvale, NJ

07465-1737

6. NOTES

6.1 Acronyms

BIT	built-in test
CCA	circuit card assembly
COTS	commercial off-the-shelf
CPU	central processing unit
DICE	Data Integrated Collection Environment
EEPROM	electrically erasable programmable read only memory
EPROM	electrically programmable read only memory
ESD	electrostatic discharge
FPGA	field programmable gate array
GFE	government furnished equipment
PC	personal computer
PLUM	PROM-based local universal monitor
PN	part number
PSP	programmable signal processor
ROM	read only memory
SRAM	static random access memory
UV	ultra violet
VME	VersaModule Europe
ZIF	zero insertion force